We CLAIMS:

sub a1

~~1. A method of accessing values stored in a cache used by a processor of a computer system, comprising the steps of:~~

~~loading a plurality of memory blocks from a memory device connected to the processor via a system bus into respective cache lines of the cache;~~

~~writing address tags associated with the memory blocks into first and second cache directories of the cache; and~~

~~reading a first memory block from the cache using the first cache directory, while reading a second memory block from the cache using the second cache directory.~~

~~2. The method of Claim 1 wherein the first and second cache directories are redundant, and said writing step writes a given one of the address tags to a specific line of the first directory and to a specific line of the second directory that corresponds to the specific line of the first directory.~~

3. The method of Claim 1 wherein the cache has a single cache entry array, and said step of reading the first memory block while reading the second memory block includes the steps of:

constructing a first control signal for the first memory block based on a first location in the first directory of an address tag associated with the first memory block;

applying the first control signal to a first multiplexer having inputs connected to the cache entry array;

constructing a second control signal for the second memory block based on a second location in the second directory of an address tag associated with the second memory block; and

applying the second control signal to a second multiplexer having inputs connected to the cache entry array.

4. The method of Claim 1 wherein the cache has first and second cache entry arrays, and said step reading the first memory block while reading the second memory block includes the steps of:

constructing a first control signal for the first memory block based on a first location in the first directory of an address tag associated with the first memory block;

applying the first control signal to a first multiplexer having inputs connected to the first cache entry array;

constructing a second control signal for the second memory block based on a second location in the second directory of an address tag associated with the second memory block; and

applying the second control signal to a second multiplexer having inputs connected to the second cache entry array.

~~5. The method of Claim 1 wherein the first and second memory blocks are read in a single clock cycle of the processor.~~

subA2

~~6. The method of Claim 2 wherein each of the first and second cache directories have a plurality of congruence classes each having a plurality of lines for storing the address tags, and said step of the processor reading the first memory block while the system bus is reading the second memory block includes the steps of:~~

~~associating a first requested address with a first congruence class in the first cache directory;~~

~~comparing each of the address tags stored in the first congruence class with a portion of the first requested address;~~

~~associating a second requested address with a second congruence class in the second cache directory; and~~

~~comparing each of the address tags stored in the second congruence class with a portion of the second requested address.~~

6 ~~7~~. The method of Claim 3 wherein the first cache directory is connected to a first interconnect on a processor side of the cache, and the second cache directory is connected to a second interconnect on a system bus side of the cache, and said step of reading the first memory block while reading the second memory block further includes the steps of:

presenting the first memory block to the first interconnect by connecting the first interconnect to an output of the first multiplexer; and

presenting the second memory block to the second interconnect by connecting the second interconnect to an output of the second multiplexer.

~~8~~ 7. The method of Claim 4 wherein the first cache directory is connected to a first interconnect on a processor side of the cache, and the second cache directory is connected to a second interconnect on a system bus side of the cache, and said step of reading the first memory block while reading the second memory block further includes the steps of:

presenting the first memory block to the first interconnect by connecting the first interconnect to an output of the first multiplexer; and

presenting the second memory block to the second interconnect by connecting the second interconnect to an output of the second multiplexer.

~~9~~ 5. The method of Claim ~~6~~ 2 wherein, if an error occurs when examining a particular address tag as part of said step of comparing the address tags stored in the first congruence class, then a redundant address tag is substituted for the particular address tag by examining a line of the second cache directory which corresponds with the line in the first cache directory containing the particular address tag.

sub a3

~~10. A computer system comprising:~~

~~a processor;~~

~~a memory device;~~

~~a system bus connected to said memory device;~~

~~a cache having a plurality of cache lines for storing memory blocks corresponding to addresses of said memory device; and~~

~~means for simultaneously reading a first memory block from said cache and reading a second memory block from said cache.~~

~~11. The computer system of Claim 10 wherein said simultaneous reading means includes first and second cache directories.~~

~~12. The computer system of Claim 10 wherein said simultaneous reading means reads said first memory block and said second memory block in a single clock cycle of said processor.~~

~~13. The computer system of Claim 11 wherein said first and second cache directories are redundant, and further comprising means for writing an address tag of a memory block which is stored in said cache to a specific line of said first cache directory and to a specific line of said second directory that corresponds to said specific line of said first cache directory.~~

Sub a4

~~14. The computer system of Claim 11 wherein said cache has a single cache entry array, and said simultaneous reading means includes means for:~~

~~constructing a first control signal for said first memory block based on a first location in said first directory of an address tag associated with said first memory block;~~

~~applying said first control signal to a first multiplexer having inputs connected to said cache entry array;~~

~~constructing a second control signal for said second memory block based on a second location in said second directory of an address tag associated with said second memory block; and~~

~~applying said second control signal to a second multiplexer having inputs connected to said cache entry array.~~

~~15. The computer system of Claim 11 wherein said cache has first and second cache entry arrays, and said simultaneous reading means includes means for:~~

~~constructing a first control signal for said first memory block based on a first location in said first directory of an address tag associated with said first memory block;~~

~~applying said first control signal to a first multiplexer having inputs connected to said first cache entry array;~~

~~constructing a second control signal for said second memory block based on a second location in said second directory of an address tag associated with said second memory block; and~~

~~applying said second control signal to a second multiplexer having inputs connected to said second cache entry array.~~

~~16. The computer system of Claim 11 wherein each of said first and second cache directories have a plurality of congruence classes each having a plurality of lines for storing said address tags, and said simultaneous reading means further includes means for:~~

~~associating a first requested address with a first congruence class in said first cache directory;~~

~~comparing each of said address tags stored in said first congruence class with a portion of said first requested address;~~

~~associating a second requested address with a second congruence class in said second cache directory; and~~

~~comparing each of said address tags stored in said second congruence class with a portion of said second requested address.~~

12 ~~17~~. The computer system of Claim 9 ~~14~~ further comprising a first interconnect for communicating with said processor, and a second interconnect for communicating with said system bus, and wherein said simultaneous reading means further includes means for:

presenting said first memory block to said first interconnect by connecting said first interconnect to an output of said first multiplexer; and

presenting said second memory block to said second interconnect by connecting said second interconnect to an output of said second multiplexer.

13 ~~18~~. The computer system of Claim 10 ~~15~~ further comprising a first interconnect for communicating with said processor, and a second interconnect for communicating with said system bus, and wherein said simultaneous reading means further includes means for:

presenting said first memory block to said first interconnect by connecting said first interconnect to an output of said first multiplexer; and

presenting said second memory block to said second interconnect by connecting said second interconnect to an output of said second multiplexer.

14 ~~19~~. The computer system of Claim 11 ~~16~~ wherein, if an error occurs when examining a particular address tag as part of said comparing of said address tags stored in said first congruence class, then a redundant address tag is substituted for said particular address tag by examining a line of said second cache directory which corresponds with a line in said first cache directory containing said particular address tag.